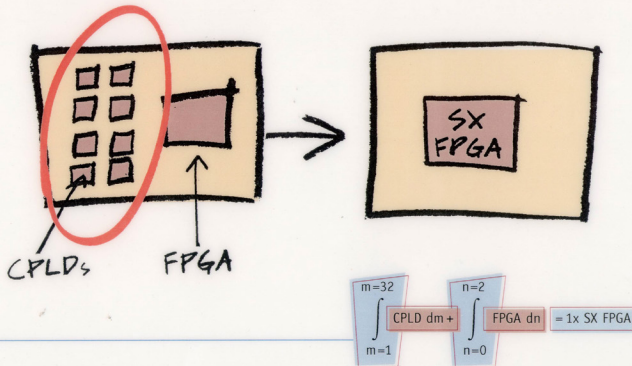


How you can integrate up to 32 CPLDs into a single high-performance FPGA.



As FPGAs and CPLDs have become larger, faster and more complex, they've taken on more important, dedicated functions and consolidated many standard parts. PC boards have been miniaturized, and individual boards have been created to replace entire systems.

As this trend continues, Actel can show that, when considering high frequencies and using fast CPLDs, the SX FPGA can both improve performance and save up to 75 percent of your component costs and power consumption.

Next time, give yourself a break. Consider the SX alternative.

The SX FPGA, with up to 64,000 gates, boasts a clock-to-out (pin-to-pin) of 4.0 ns and a pin-to-pin delay for 32-bit decode of 7.7 ns, demonstrating the ability to integrate multiple CPLDs and save on component costs, board space and power consumption ... improving performance at the same time.

The performance boost comes in part from Actel's highly usable "Sea of Modules" architecture, which combines small, synthesis-friendly logic building blocks with fast and predictable local and general routing resources.

Performance issues aren't limited to nanoseconds and megahertz, but time-to-market and the nights spent grinding the design through synthesis and simulation tools. With SX, getting high performance is easy. Why? The intrinsic speed of the SX FPGAs promotes successful integration of performance-intensive designs.

As you collapse a lot of functions into one chip, complexity increases logarithmically, so take the next step in the cycle. Simplify your system design, and your life, by integrating with an FPGA that has the performance, the size and the design environment to make it as easy as possible. The Actel SX FPGA.

For detailed information on how the SX FPGA can integrate multiple CPLDs in your design, call 1-888-99ACTEL or visit www.actel.com