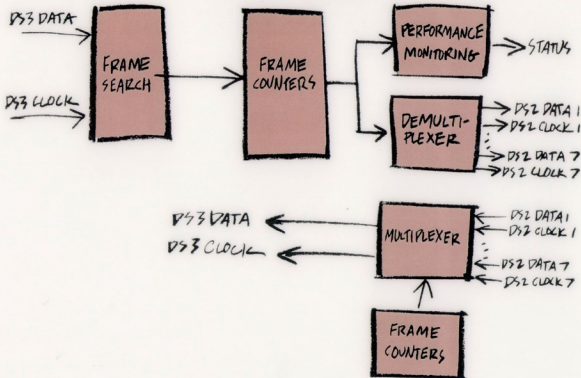


How 4.0 ns clock-to-out and fast internal logic enabled a DS2 to DS3 bi-directional converter for high-speed telecom.

ADA BLOCK DIAGRAM



19.2 ns REGISTER-REGISTER!!

A telecommunications company with industry-leading technology wanted to implement a bi-directional converter in programmable logic.

The circuit had to convert between the DS2 and DS3 telecommunications standard at the maximum DS3 bit rate of 45 Mbits per second. With additional control characters, the maximum operating frequency is actually 52 Mhz, a transfer rate that required the programmable logic to run at 19.2 ns, register-to-register.

Problem was, no programmable logic vendor they were familiar with

was able to operate at 19.2 ns, register-to-register, with this design.

The company then asked Actel to benchmark the design on the SX FPGA and found that it was able to operate the converter at 15 ns register-to-register. Beating their performance goals and getting their design to market faster.

For detailed information on how the SX can integrate multiple CPLDs in your design, call 1-888-99ACTEL or visit www.actel.com