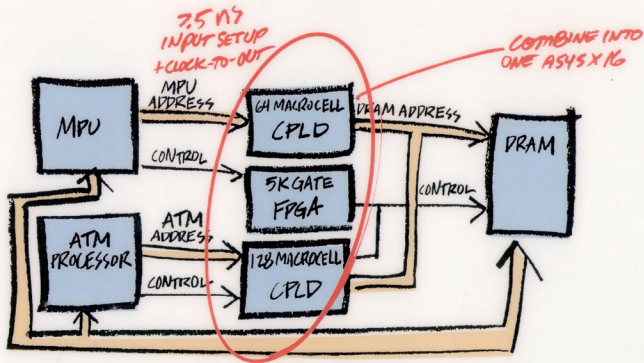


How a single SX replaced two power-hungry CPLDs and an FPGA to save cost, power and board space in a high-speed, synchronous DRAM controller application.



Designers frequently use multiple high-speed CPLDs to integrate the addressing and control of DRAM chips. However, increasing system speeds demand the fastest CPLDs, which carry a high power consumption penalty; this conflicts with shrinking power budgets as system miniaturization proceeds. Actel's SX FPGAs allow for the integration of multiple high-speed CPLDs into a single FPGA, saving power, cost and board space without sacrificing performance.

The 0.6 ns input setup time and 4.4 ns clock-to-out (pin-to-pin) of the Actel SX A54SX16 were ample to permit integration of multiple CPLDs and an FPGA in this high-speed application.

The SX saved on component costs, board space, power consumption and heat dissipation while beating the 7.5 ns input setup plus clock-to-output pin-to-pin timing required to successfully address the high-speed, synchronous DRAM in a high-end, data networking application.

For detailed information on how the SX can integrate multiple CPLDs in your design, call 1-888-99ACTEL or visit www.actel.com